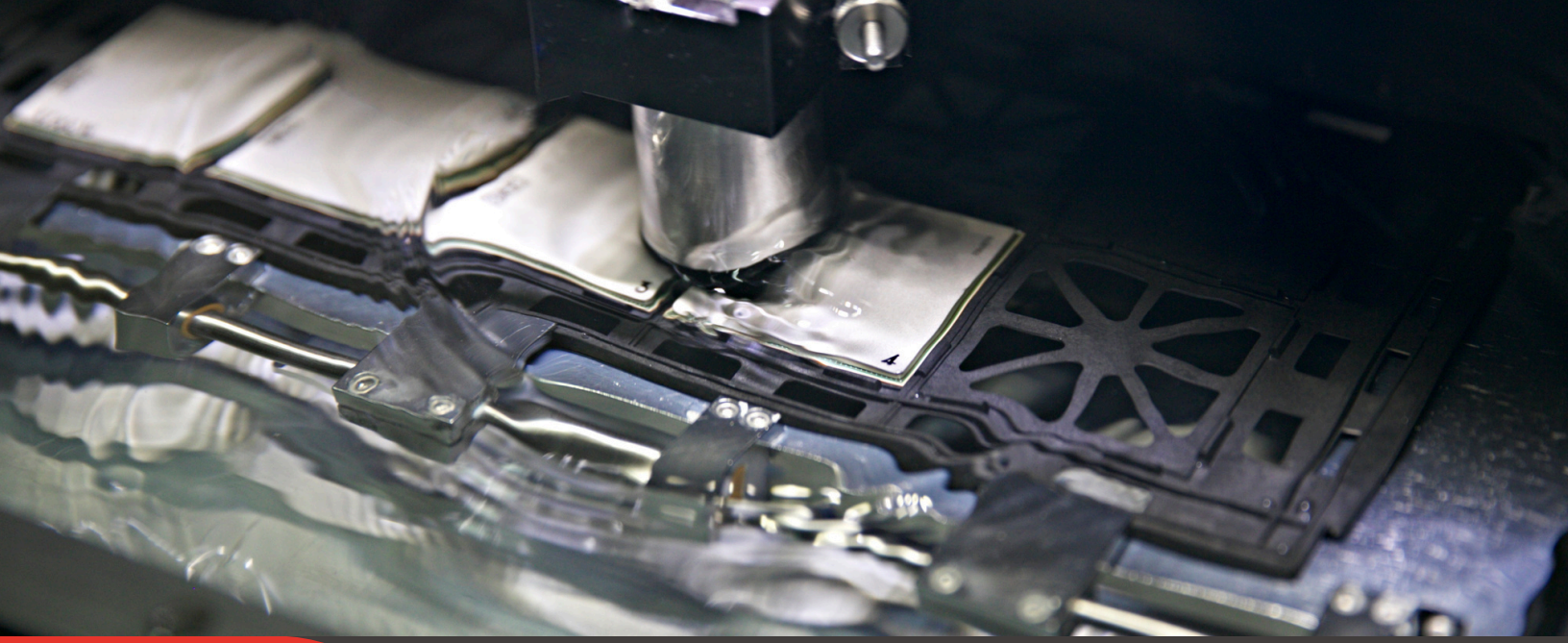

FAILURE ANALYSIS: FROM DETECTION TO SOLUTIONS.

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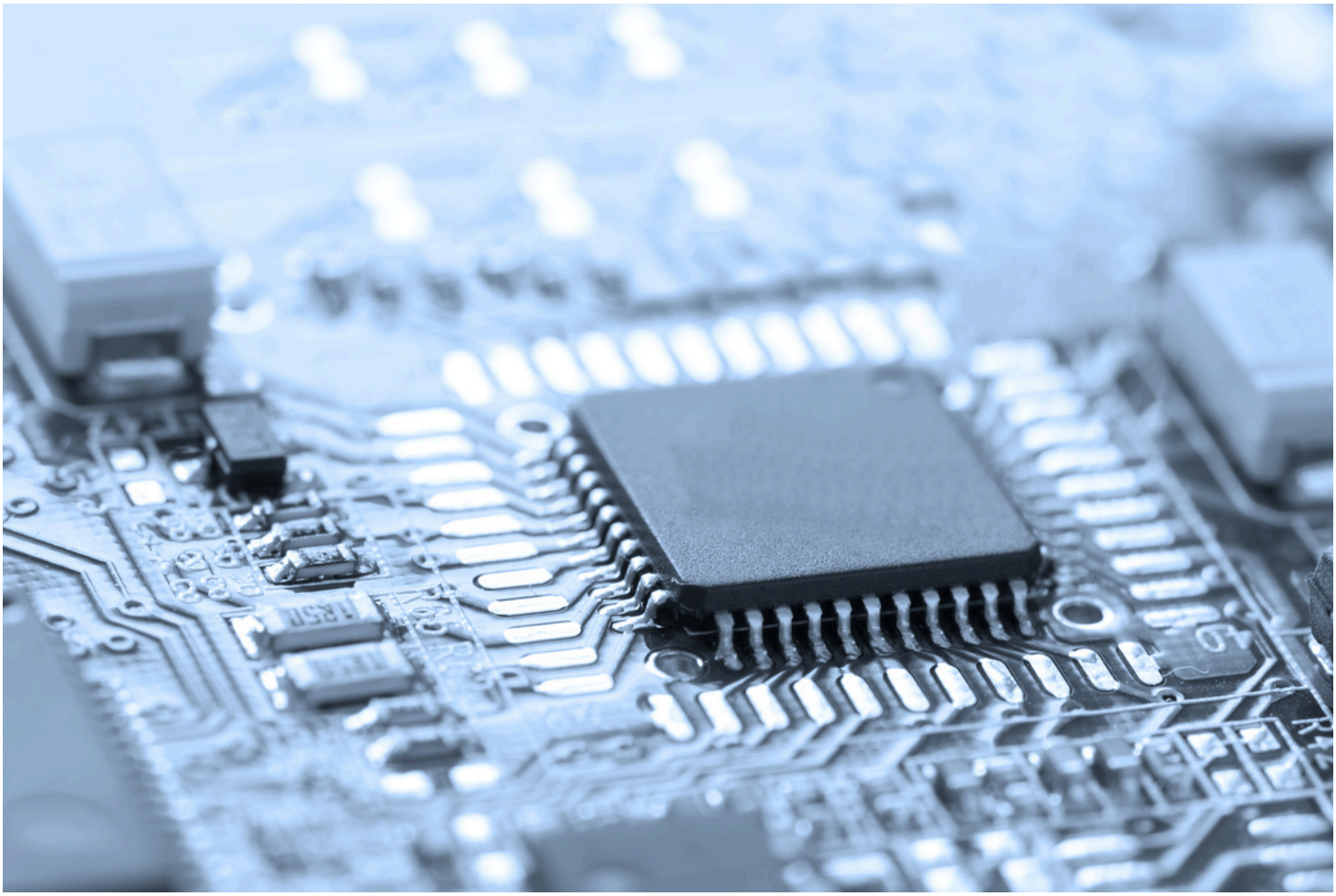
OCTOBER 2025

1. INTRODUCTION

Failure analysis constitutes an essential systematic process in the semiconductor field, aimed at identifying the root cause of a malfunction within an electronic system or component. The increasing complexity of integrated structures makes this approach particularly demanding, especially regarding the preservation of evidence related to the failure mechanism.

The adoption of a rigorous methodology is therefore crucial to ensure product quality and reliability, while facilitating the implementation of targeted and effective corrective solutions. By enabling precise identification of the problem root cause, failure analysis contributes to optimizing resources and reducing resolution timeframes.

This article provides an overview of the failure analysis process applied to assembled and encapsulated modules available at the C2MI laboratory.



2. TYPES OF FAILURES IN ELECTRONIC CHIP ENCAPSULATION

Electronic devices can exhibit various types of failures. In assembled modules, the most common modes are open circuits, short circuits, and intermittent failures.

Open circuits are generally caused by interconnection defects, such as:

- Interconnection fatigue induced by thermal cycling (Figure 1).
- Poor interconnection bonding during assembly on the substrate (Figure 2).

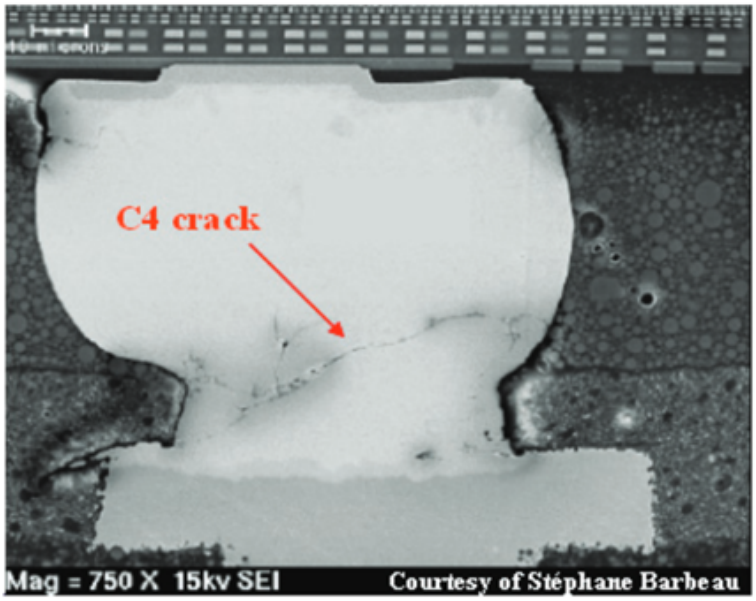


Figure 1: Crack in the interconnection (Controlled Collapse Chip Connection "C4") [1].

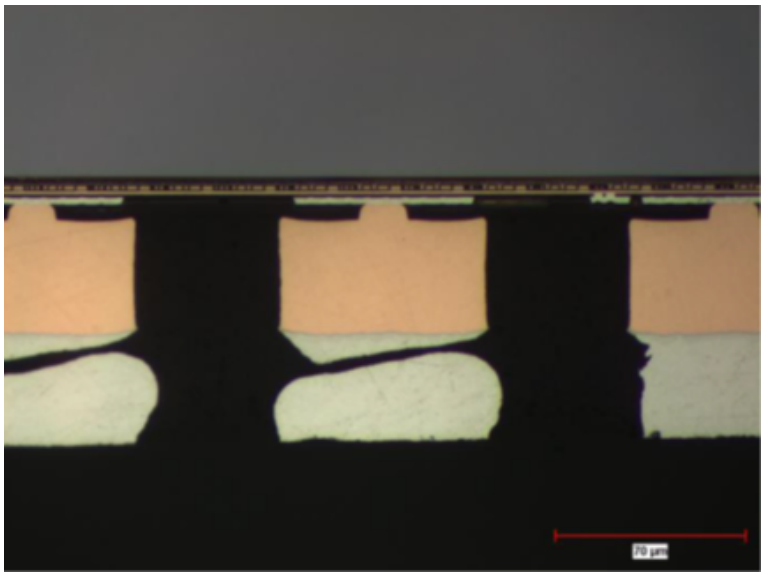


Figure 2: Micro-section of an open circuit from poor adhesion (non-wet) of an interconnection.

At the substrate level, open circuits can result from manufacturing defects, thermomechanical stress (warpage), or cracks in inter-layer vias (Figure 3).

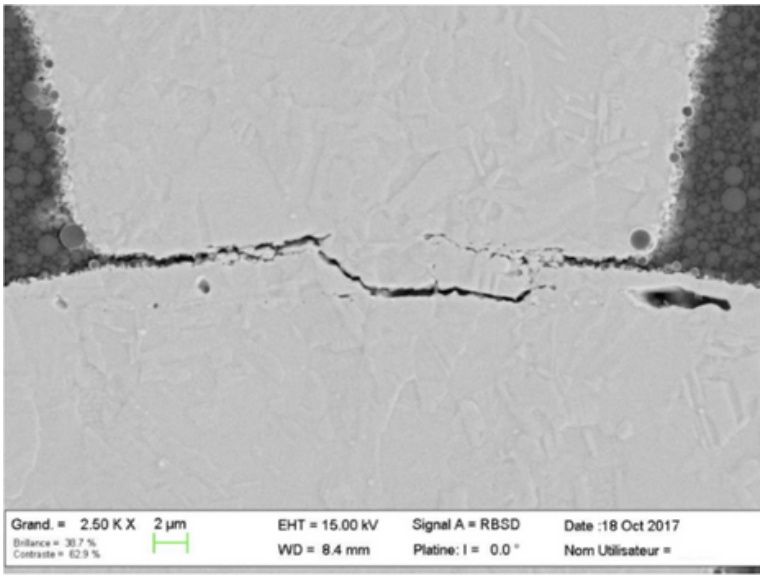


Figure 3: Micro-section of an intermittent open circuit observed in a laminate via.

Short circuits correspond to unwanted connections between two electrical signals. They can, for example, be caused by:

- Bridges between interconnections.
- Excess metal on the laminate.
- Conductive contaminants (Figure 4).
- Defects in encapsulation materials, such as voids in the underfill promoting solder extrusion during board attachment.

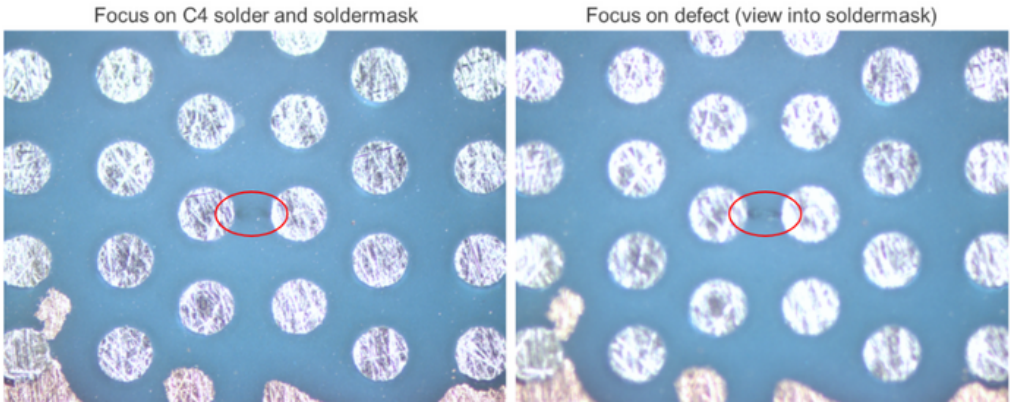


Figure 4: Z-section down to the substrate protective layer ("soldermask") of contamination between 2 electrical signals in the encapsulation matrix ("underfill").

Finally, **delayed failures**, which are rarer and more difficult to diagnose, can occur. They are generally related to evolutionary phenomena such as **electromigration** or environment-induced **corrosion**, progressively affecting system performance.

3. FAILURE ANALYSIS PROCEDURE

The failure analysis process is methodical and enables obtaining the maximum amount of information possible to help find the root cause of the failure. It is divided into 4 main steps (Figure 5):

1. Electrical validation of the failure
2. Initial inspection and sample preparation
3. Iterative process of sample delayering and failure characterization
4. Failure report

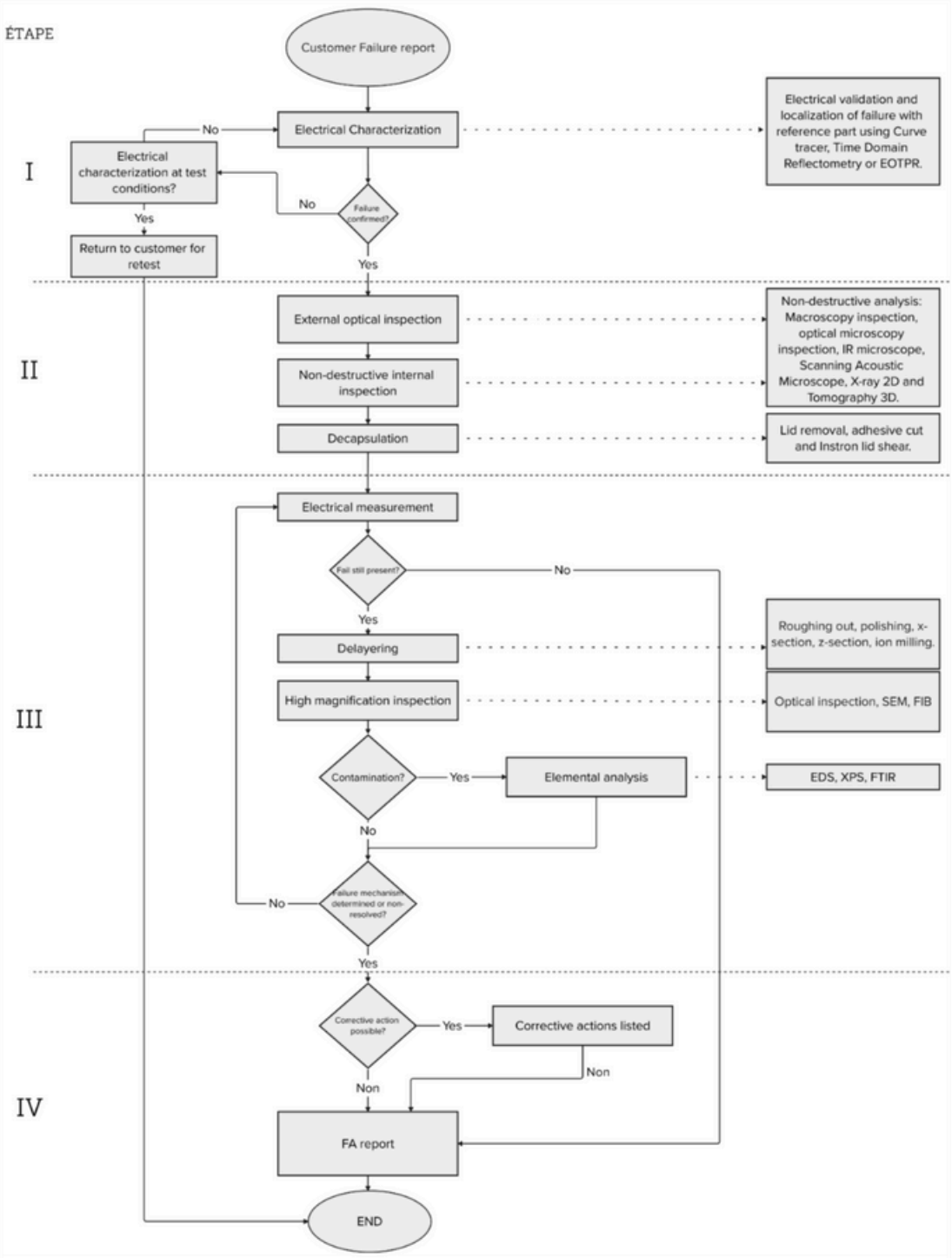


Figure 5: Detailed failure analysis process, inspired by Pabbisetty, 1999 [2].

4. ELECTRICAL TESTING METHODS

In the context of failure analysis of assembled electronic modules, electrical tests performed in the laboratory do not have the same capabilities as Automated Test Equipment (ATE), which enables comprehensive validation of integrated circuit electrical functionality.

In failure analysis context, continuity tests – primarily short-circuit and open-circuit tests – are performed using manual measurement stations. These tests aim to detect elementary electrical anomalies in the interconnections or module components.

To improve spatial localization of defects, the use of Time Domain Reflectometry (TDR) is recommended. This technique enables more precise identification of the position of discontinuities in transmission lines or internal interconnections.

The results obtained from these electrical measurements constitute a critical step to confirm the nature of the observed failure. They guide the analysis strategy to be adopted during delamination operations, by maximizing the preservation of physical evidence likely to corroborate the failure mechanism.

5. INSPECTION TECHNIQUES

Initial observations constitute an essential step in the macroscopic characterization of electronic modules, enabling identification of potential deviations between a reference part and a failed part. From the earliest phases of failure analysis, the optical microscope emerges as the preferred tool. At different magnification levels, it provides relevant information both in preliminary analysis and during successive destructive delayering steps.

In direct comparison with a reference part, optical observations enable detection of morphological or structural variations. When an anomaly is suspected, increased magnification or the use of Scanning Electron Microscopy (SEM) is performed to obtain high-resolution surface imaging. SEM also enables fine characterization of defect morphology and, coupled with Energy Dispersive X-ray Spectroscopy (EDS), offers localized chemical analysis capability.

Complementary non-destructive techniques are also used. The Scanning Acoustic Microscope (SAM) enables detection of delaminations and porosity at different critical interfaces of the module through either reflection or transmission of ultrasonic waves. The infrared microscope, meanwhile, is effective for detecting cracks in silicon integrated circuits.

X-ray imaging enables visualization of internal structures, particularly BGA-type solder joints and defects present in denser materials. X-ray tomography constitutes an advanced technique enabling volumetric reconstruction of inspected objects, particularly useful for analyzing complex internal defects.

6. DELAYERING TECHNIQUES

The delayering strategy is adjusted based on results obtained through various non-destructive inspection techniques. These observations enable targeting areas of interest and selecting the most appropriate method to access internal layers or defects.

1. **Mechanical sawing**
   - Used for rough cuts or to quickly access a specific area.
2. **X-section polishing (cross-section)**
   - Enables observation of stacked layers in the horizontal plane.
   - Useful for multilayer structures or interfacial defects.
3. **Z-section polishing (depth)**
   - Used to reveal successive layers in depth.
   - Often employed for sequential or 3D analyses.
4. **Ion Milling**
   - Precision technique to refine and reveal microstructures of mechanically polished surfaces without further damaging structures.
   - Ideal for sensitive materials or critical areas.
5. **FIB cuts (Focused Ion Beam)**
   - Very high precision enables targeting microscopic areas.
   - Enables layer exposure without causing any polishing artifacts.
   - Used for local analyses, coupled with SEM for alignment and observation.

7. CHEMICAL CHARACTERIZATION

Chemical characterization plays an essential role in identifying the nature of contaminations likely to have caused a failure. By determining the chemical composition of contaminations, it becomes easier to understand the origin of the problem, propose targeted corrective actions, and prevent future recurrences.
The different analytical techniques used in chemical characterization notably include **EDS**, **XPS**, and **FTIR**:

1. **EDS (Energy Dispersive X-ray Spectroscopy):**
   - Coupled with SEM.
   - Enables local elemental analysis.
   - Fast and semi-quantitative.
2. **XPS (X-ray Photoelectron Spectroscopy):**
   - Analysis of surface chemical states.
   - Very useful for thin films or surface contaminations.
   - Provides information on chemical bonds.
3. **FTIR (Fourier Transform Infrared Spectroscopy):**
   - Identification of organic compounds.
   - Very effective for polymeric residues or organic contaminations.
   - Spectroscopy based on molecular vibrations.

8. CASE STUDY

The customer reported an intermittent open circuit failure affecting multiple modules. Although the electrical station and TDR confirmed the presence of a single intermittent open circuit, once the package was removed from the module, anomalies were observed in 3D tomography in the via stacks of the organic substrate (Figure 6).

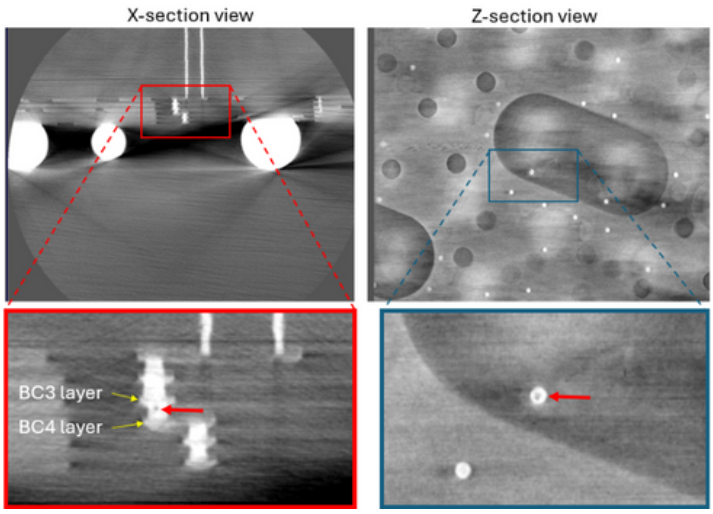


Figure 6: 3D tomography observation in x-section and z-section of the void defect in the laminate via stack.

The delayering and mechanical polishing of the laminate enabled revealing the defect of interest. Inspection under high magnification optical microscope then enabled better visualization and characterization of this defect (Figure 7).

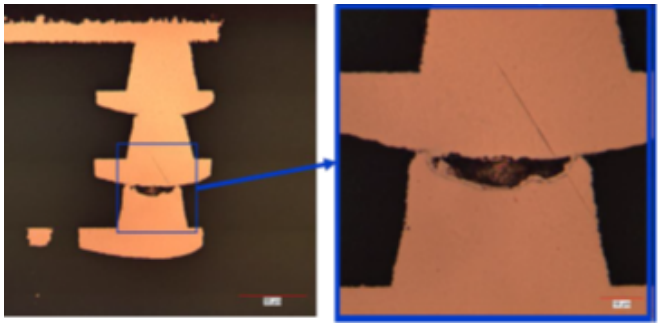


Figure 7: Observation under high magnification optical microscope.

After ion milling, the copper microstructure as well as artifacts related to mechanical polishing could be observed in detail under SEM (Figure 8). The FIB cross-section also confirmed the presence of a void, with no trace of residual contamination (Figure 9).

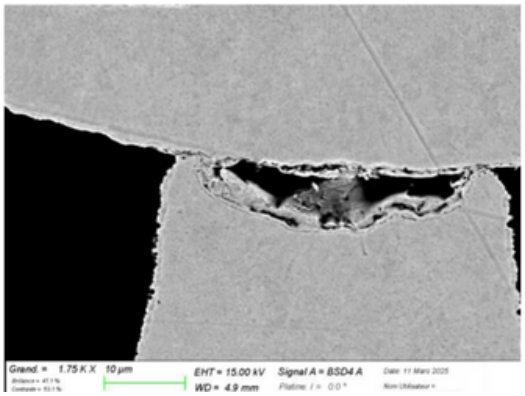


Figure 8: SEM observation of the defect following ion milling.

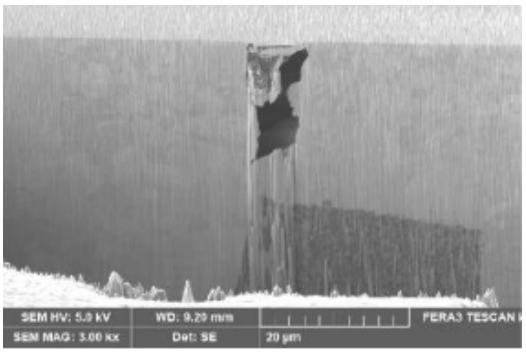


Figure 9: Observation of the FIB cross-section of the defect.

A corrective action was implemented with the organic laminate supplier to prevent recurrence of this type of failure.

9. CONCLUSION

Failure analysis occupies a central place in the semiconductor industry due to the increasing complexity of devices and ever-stricter reliability requirements. It is not limited to identifying root causes of failures: it constitutes a strategic lever to improve manufacturing processes, reduce costs related to customer returns, and guarantee product quality in a highly competitive market.

Beyond its corrective role, failure analysis is a driver of innovation. By providing precise information on failure mechanisms, it feeds the design of new structures, material optimization, and process improvement. This continuous learning loop not only increases device reliability and performance but also accelerates the development of advanced assembly technologies such as: sub-5 nm nodes, 3D devices, and solutions for artificial intelligence (AI) and the Internet of Things (IoT).

In summary, failure analysis is not simply a support function: it is an essential pillar of competitiveness and technological sustainability in the semiconductor industry.

The C2MI team offers expertise and execution of failure analyses. Our experts can develop a customized analysis plan to find the root cause of various failures in your products, whether in development or production. Contact our team to learn more.

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[1] M.-C. Paquet, J. Sylvestre, E. Gros, et N. Boyer, « Underfill delamination to chip sidewall in advanced flip chip packages », dans 2009 59th Electronic Components and Technology Conference, mai 2009, p. 960-965. doi: 10.1109/ECTC.2009.5074129.

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